Evaluation of Analog Parameters in SOI Nanowires nMOSFETs

Vinícius Rodrigues Prates and Michelly de Souza
Electrical Engineering Department, Centro Universitário FEI, São Bernardo do Campo, Brazil
unievprates@fei.edu.br, michelly@fei.edu.br

***Abstract*— This paper presents an analysis of analog parameters of SOI nanowires nMOS transistors through experimental data and numerical simulations results. The transconductance, output conductance and voltage gain are shown for different channel lengths and widths, for transistor biased at different gate and drain biases.**

Keywords—nanowire transistors, SOI, electrical characterization, 3D numerical simulations

I. INTRODUCTION

Increase of transistors density in a chip is one of the main goals in the semiconductor industry, since it can have a lot of benefits in the devices performance [1]. The principal way to reach this is by reducing the dimensions of the transistors. However, some effects appear in the transistors when the dimensions are tiny, called Shorts Channel Effects (SCE), such as threshold voltage and subthreshold slope degradation [2]. One way to circumvent these effects is the use of multiple-gate SOI transistors [3], such as the nanowire transistors. A schematic representation of a nanowire transistor is presented in Fig. 1. Due to the structure of Nanowires, which have the terminal of gate also at the sides of the channel, not only at the top like in planar MOSFETs, these undesirable effects diminish [3]. This improvement happens because of the great electrostatic control that the gate has over the channel, which reduces the influence of drain and source regions.

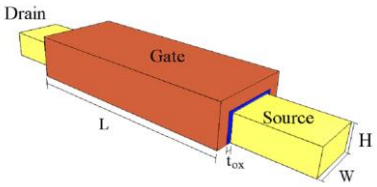

Fig. 1. Schematic view of a nanowire transitor.

The reduction of SCE in nanowires also improves the analog parameters, mainly the output conductance, which presents much lower values compared to planar SOI MOSFETs. Therefore, this paper analyzes three important analog parameters: transconductance (G_M), output conductance (G_D) and the intrinsic voltage gain (A_V). The influence of nanowire width and length over these three parameters will be analyzed at different bias conditions, including subthreshold operation. The analysis is performed by means of 3D numerical simulations and experimental results.

II. THREE-DIMENSIONAL NUMERICAL SIMULATIONS

Three dimensions numerical simulations using the Sentarus Device Simulator [4] were performed. Five models were considered: *IALMob*, to consider mobility degradation in inversion layers; *Enormal*, that considers attraction of carriers in the interface of silicon and oxide with transversal electric field; *HighFieldSaturation*, that consider the effect of high electric field on the mobility; *DopingDep*, accounts for defects in the structure of the crystalline network; *OldSlotBoom*, that considers bandgap narrowing.

All devices were simulated at temperature of 300 K, with an oxide thickness (t_{ox} in Fig. 1) of 1.3 nm, channel doping of $1x10^{15}$ cm^{-3} and a source and drain doping of $5x10^{20}$ cm^{-3} and with channel height (H) of 9 nm. The width (W_{FIN}) has been varied between 10 and 20 nm (with length fixed in 20 nm and 40 nm), and length (L) between 20 and 100 nm (with width fixed in 10 nm and 20 nm). For each simulated transistor I_D x V_{GS} with V_{DS} = 0.5 V to 1 V with step of 100 mV and I_D x V_{DS} with V_{OV} = $V_{GS} - V_t$ = -0.1 V to 0.2 V with step of 100 mV were simulated. The threshold voltage (V_t) was extracted individually using the double derivative method.

Figure 2 shows the I_D vs V_{GS} for six different drain voltages. Two transistors are shown: one with narrow and long channel (W_{FIN} = 10 nm and L = 100 nm) and other with large and short channel (W_{FIN} = 20 nm and L = 20 nm). As can be seen, I_D increases with the increase of V_{GS}, but the large and short channel device has a considerable increase before V_t, showing the loss of channel control by the gate. Furthermore, this transistor presents larger difference in the I_D curves in saturation with the V_{DS} change in comparison to the narrow and long device, something that is not supposed to happen, since in a first approximation I_D does not depend on V_{DS}.

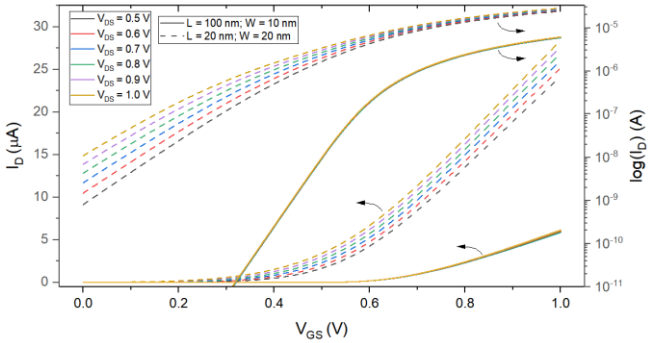

Fig. 2. I_D as a function of V_{GS}.

A. Transconductance (G_M)

The transconductance defines the efficiency of the gate voltage (V_{GS}) to control the drain current (I_D) [5]. It is mathematically defined as the derivative of I_D by V_{GS}. In saturation, the G_M is defined by the equation 1.

$$G_M = \mu_e C_{ox} V_{ov} W / L \quad (1)$$

Figure 3 presents the transconductance vs. V_{GS} obtained from the derivative of the curves presented in Figure 2. The G_M vs. W_{FIN} with V_{DS} = 0.8 V and V_{OV} = 0.1 V is presented in Figure 4(A) for two channel lengths, 20 nm and 40 nm. From these results it is possible to see the linear increase of G_M, but with different slopes for different values of channel length, having the longer one a smaller slope, 1.48 μA/V.nm and 1.04 A/V.nm for L = 20 nm and 40 nm, respectively. The results of G_M as a function of L with the same polarization of V_{DS} = 0.8 V and V_{OV} = 0.1 V is presented in Figure 4(B). As can be seen, the transconductance increase highly with the decrease of the length, but the narrower channel presents smaller increase in G_M value.

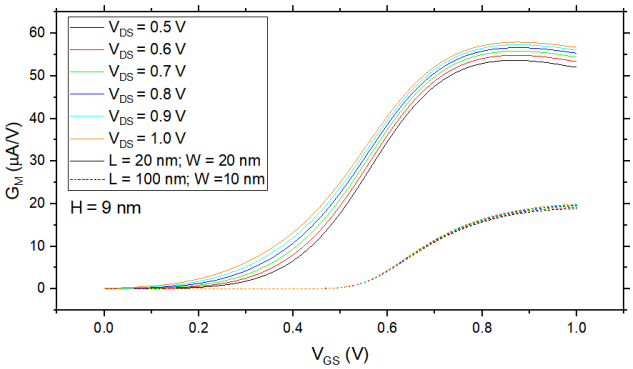

Fig. 3. G_M as a function of V_{GS}.

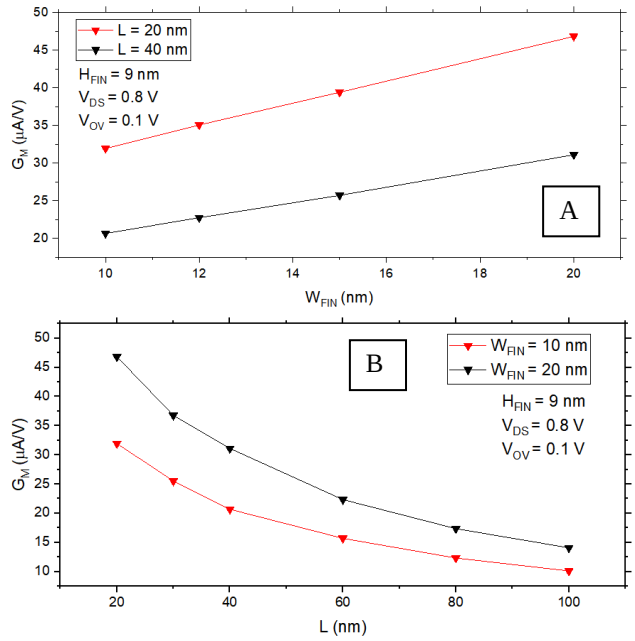

Fig. 4. G_M as a function of W_{FIN} (A) and L (B).

B. *Output Conductance (G_D)*

The conductance defines the variation of drain current with drain voltage (V_{DS}), i. e. the derivative of I_D by V_{DS} [5]. Ideally, the G_D is zero in saturation, however, due to channel length modulation (CLM), a short channel effect, the I_D increases with the drain voltage. The G_D can be described in saturation by the equation 2. As can be seen, G_D depends of the lambda parameter, but in nanowires devices this parameter is small, decreasing this parameter, becoming closer to the ideal.

$$G_D = \mu_e C_{ox} V^2_{ov} \lambda W / 2L \quad (2)$$

The G_D as a function of V_{DS} with four gate voltages is shown in Figure 5, for the same devices shown in Figure 3. For both transistors G_D is different from zero, because of CLM. However, the transistor with narrow and long channel presents lower value of G_D, showing less shorts channel effects in this transistor. The curves of G_D as a function of W_{FIN} and L are presented in Figure 6, biased at V_{DS} = 0.8 V and V_{OV} = 0.1 V. The same tendency of G_M appears with the G_D, increasing its value with the increase of W_{FIN} and the decrease of L. This happens because both parameters depend on the relation L/W.

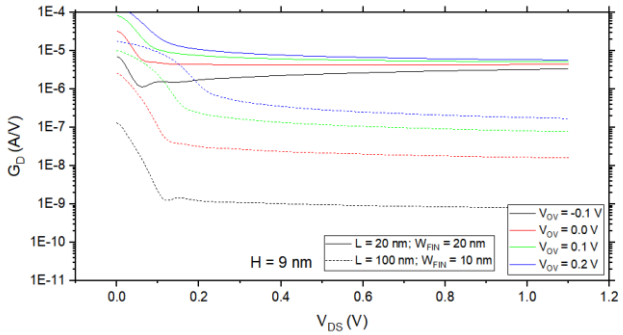

Fig. 5. G_D as a function of V_{DS}.

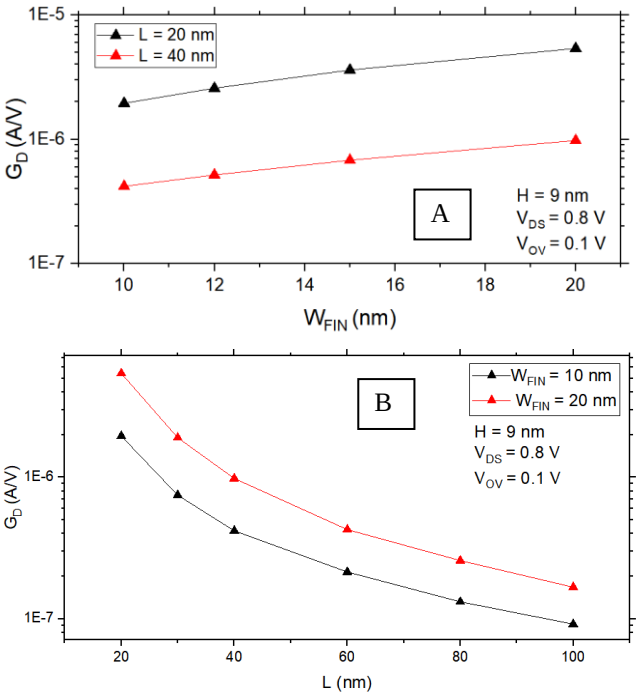

Fig. 6. G_D as a function of W_{FIN} (A) and L (B).

C. *Voltage Gain (A_V)*

The voltage gain is an essential parameter in analog circuits such as amplifiers. It defines how much the voltage varies in the output with a variation in the input of the circuit. For MOSFETs biased in common-source configuration, A_V can be expressed by equation 3 [5]. As can be seen, the A_V depends inversely of G_D, showing that shorts channel effects harm this parameter.

$$A_V = G_M / G_D \quad (3)$$

Figure 7 shows the A_V as a function of V_{DS}, obtained using the curves presented in Figures 3 and 5. It is possible to see that the transistor with narrow and long channel presents a higher value of A_V compared to the transistor of large and short channel, due to the increase of gate control over channel promoted by the nanowire narrowing reducing the conductance and by consequence increasing the voltage gain. It can also be seen that the curve of V_{OV} present different tendency for each transistor. Transistor with short and large channel presents larger value of A_V when the V_{OV} is increased, while the transistor with long and narrow channel presents larger A_V with the smallest value of V_{OV}. So, there is a trend change in the curves of A_V with the change of the dimensions.

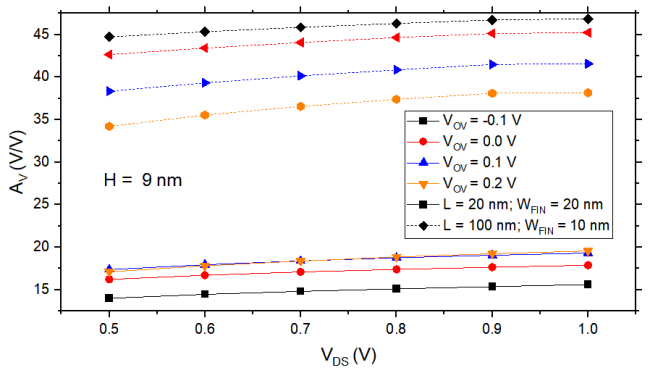

Fig. 7. A_V as a function of V_{DS}.

The Figure 8(A) shows the value of A_V vs. W_{FIN} with V_{DS} = 0.8 V and different values of V_{OV}. The highest value of voltage gain occurs with small values of W_{FIN}, due to increased electrostatic control, and increases with V_{OV} reduction, approaching the subthreshold region. However, when the W_{FIN} increases, A_V decreases and a trend inverse occurs with V_{OV} change. The same trend change can be seen in Figure 8(B), where A_V as a function of L with V_{DS} = 0.8 V and different V_{OV} is shown. However, in this curve the highest value of voltage gain occurs with high values of L (not with small values, like with the W_{FIN}). In these cases, the reduction of V_{OV} increases the A_V, while in small values of L the reduction of V_{OV} decrease the voltage gain.

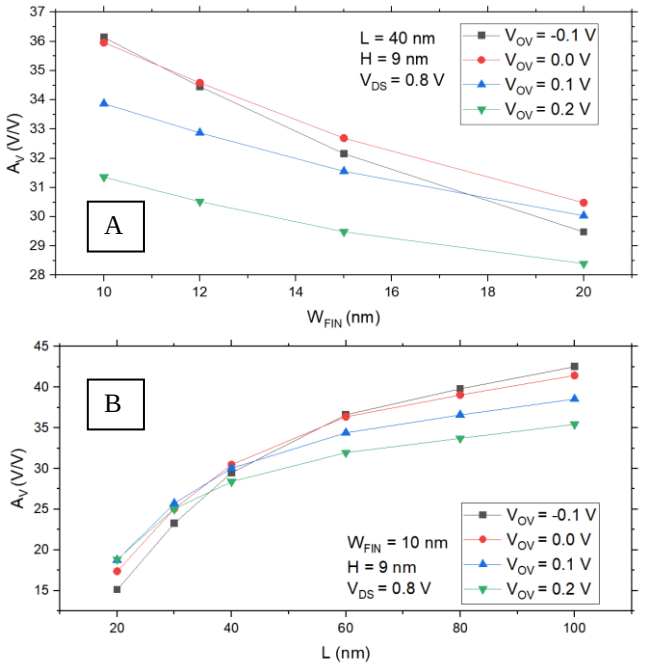

Fig. 8. A_V as a function of W_{FIN} (A) and L (B).

The presented results show that even with the transconductance the output conductance reduction with the increase of the L and the decrease of W_{FIN}, the voltage gain is benefited in these cases, indicating that G_D reduces much more than the G_M, increasing the A_V consequently.

III. Experimental Results

Electrical Measurements were made in chips produced by CEA-Leti [6]. The gate stack is composed of a thin interfacial SiO_2 layer, followed by 2.3 nm HfSiON, 5 nm TiN, and 50 nm polysilicon. The effective oxide thickness (EOT) is around 1.4 nm. The channel region is not intentionally doped. Devices present a fin height of 9 nm. The nanowire width (W_{FIN}) has been varied between 12 and 222 nm (with length fixed in 40 nm and 100 nm), and length (L) between 30 and 400 nm (with width fixed in 12 nm).

The G_M vs. V_{GS} and the G_D in function of V_{DS} are shown in the Figures 9(A) and 9(B), respectively. As in the simulation, transistors with short and large channel present bigger G_M but also a high difference in the curves with different V_{DS}. The G_D is also larger in transistors with short and large channel due to the short channel effects, as in the simulations.

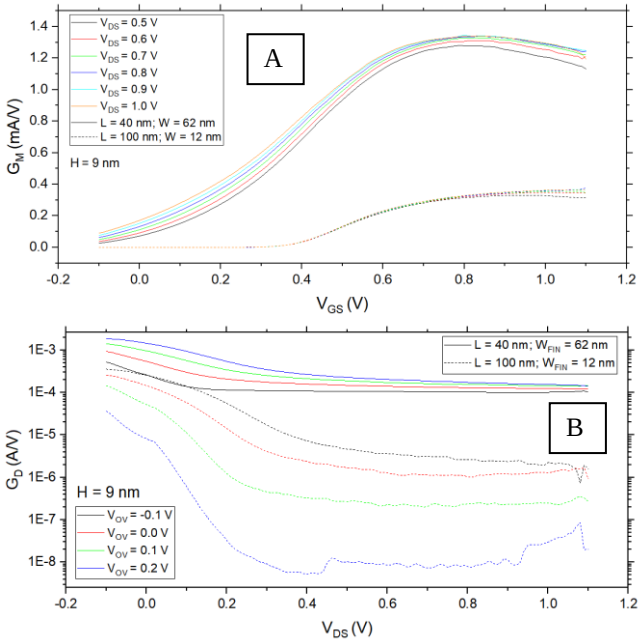

Fig. 9. Experimental curves of G_M vs. V_{GS} (A) and G_D vs. V_{DS} (B).

Figure 10 show the G_M and G_D vs. W_{FIN} for V_{DS} = 0.8 V and V_{OV} = 0.1 V and they present similar results to the simulations, having approximately a linear increase in the G_M and the G_D when the W_{FIN} increases, even with bigger values of width, which the simulation does not presents.

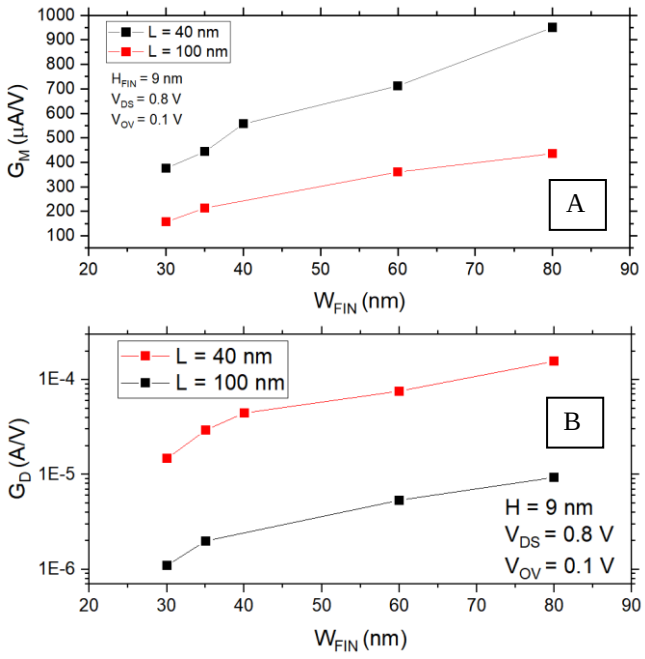

Fig. 10. Experimental results of G_M (A) and G_D (B) as a function of W_{FIN}.

The G_M and G_D vs. L with V_{DS} = 0.8 V and V_{OV} = 0.1 V is presented in Figure 11. The same tendency of increase of G_M and G_D when the L decrease appears in the experimental results, even with large values of L.

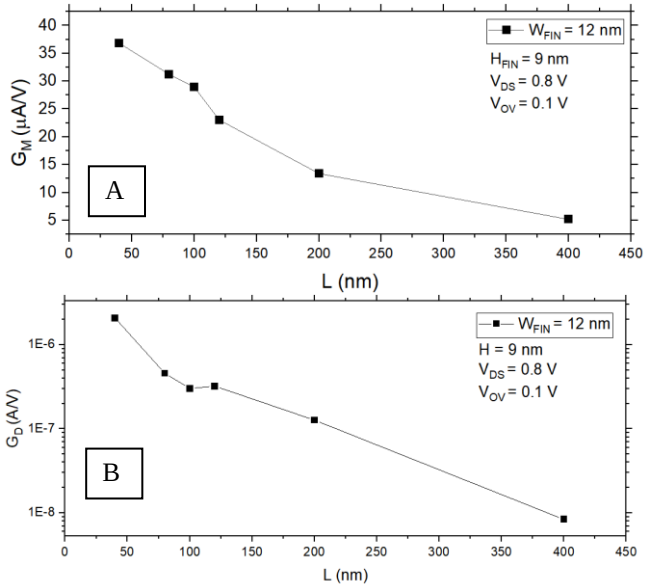

Fig. 11. Extracted values of G_M (A) and G_D (B) as a function of L.

Figure 12 shows the A_V vs. V_{DS} for two different transistors, being one with L = 200 nm and W_{FIN} = 12 nm and the other with L = 40 nm and W_{FIN} = 62 nm, both presenting four different gate bias. It can be seen difference tendencies for the two transistors: the transistor with narrow and long channel presents the higher voltage gain with the V_{OV} = -0.1 V, while the transistor with large and short channel presents a higher voltage gain with the V_{OV} = 0.2 V. Furthermore, the transistor with narrow and long channel presents a higher value for all polarization compared to the other transistor.

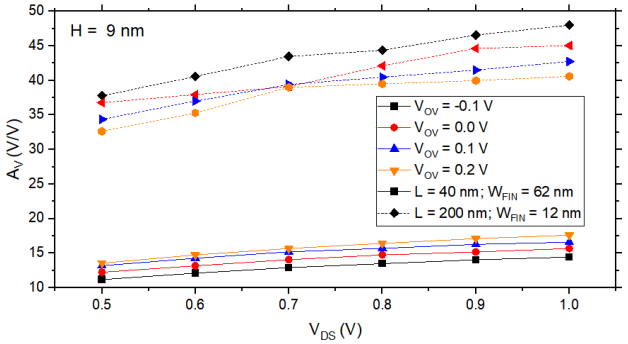

Fig. 12. A_V as a function of V_{DS}.

Figure 13 shows the A_V vs. W_{FIN} and L. It is possible to see that for small values of W_{FIN} the A_V shows a large increase and that the V_{OV} reduction increases A_V, whereas large nanowires show higher gain with larger V_{OV}.

IV. Conclusions

This paper presented the influence of nanowires transistors dimensions in analog parameters using 3D numerical simulations and electrical measurements. It was shown that the transconductance and output conductance presented the same tendency of decrease when channel length is increased and when the width is decreased. The reduction of width increases electrostatic control, improving output conductance. At the same time, transconductance reduces due to the total width reduction. An A_V increase has been observed in those cases. This happens due to the fact that the G_D reduces more than the G_M due to the structure of nanowire that improves the control of the gate over the channel, reducing the channel modulation effect. It was also shown that the voltage gain dependence on V_{OV} depends on the channel dimensions. The results showed that when the channel is long and narrow, larger gain is obtained when the transistor operates in the subthreshold region, with a negative gate voltage overdrive. When the channel is large and short, the highest A_V is reached for higher V_{OV} values. So, narrow and long channel operating in subthreshold region presents the best analog characteristics since the gain voltage is higher and presents a lower power consumption.

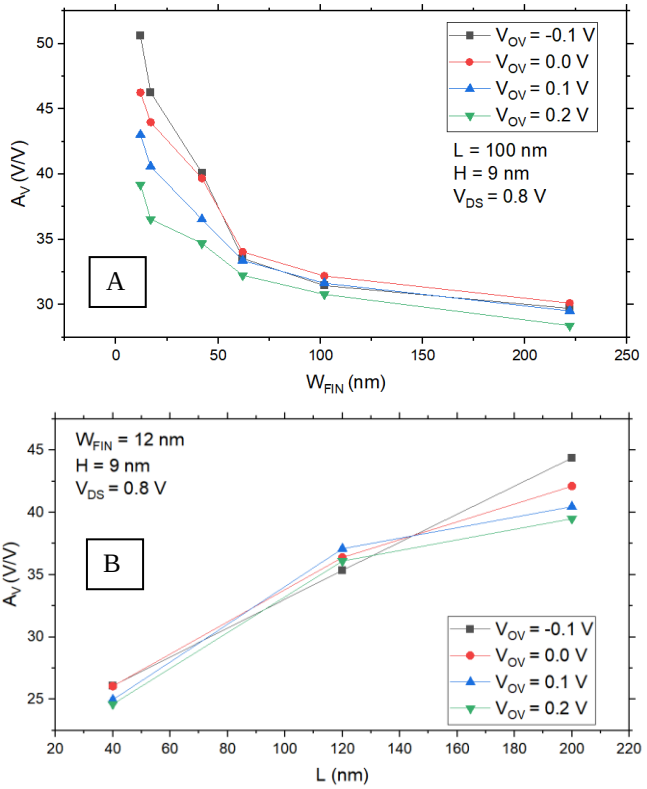

Fig. 13. Experimental A_V as a function of W_{FIN} (A) and L (B).

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